Bringing Order to the World of Nanowire Devices by Phase Shift Lithography

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S *Supporting Information*

ABSTRACT: Semiconductor nanowire devices have several properties which match future requirements of scaling down the size of electronics. In typical microelectronics production, a number of microstructures are aligned precisely on top of each other during the fabrication process. In the case of nanowires, this mandatory condition is still hard to achieve. A technological breakthrough is needed to accurately place nanowires at any specific position and then form devices in mass production. In this article, an upscalable process combining conventional micromachining with phase shift lithography will be demonstrated as a suitable tool for nanowire device technology. Vertical Si and ZnO nanowires are demonstrated on very large (several cm^2) areas. We demonstrate how the nanowire positions can be controlled, and the resulting nanowires are used for device fabrication. As an example Si/ZnO heterojunction diode arrays are fabricated. The electrical characterization of the produced devices has also been performed to confirm the functionality of the fabricated diodes.

KEYWORDS: ZnO nanowires, Si nanowires, phase shift, lithography, alignment, patterning
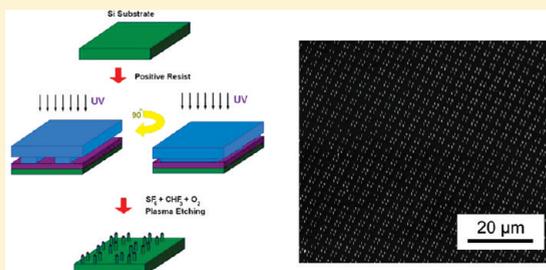
Semiconductor nanowires (NWs) are expected to be one of the alternatives for scaling down the dimensions as well as for enhancing the performance of electronic devices which represents the main driving force of this rapid developing field. Several NW-based devices were already reported demonstrating interesting thermoelectric, electronic, and even biosensing properties.[1−3] ZnO NWs are considered a good candidate for gas sensors, field effect transistors, UV-light-emitting diodes, and lasers.[4−7] Vertical semiconductor nanowires are usually grown randomly and, in most cases, lacking a defined position on the substrate. Therefore, mass production, as in the case of normal microelectronic fabrication, is hard to achieve, and until now, most device demonstrations are only based on single wires.[8] Several techniques were introduced to improve the positioning of nanowires, for instance, electron beam (e-beam) lithography, nanosphere lithography, laser interference lithography, and other template-assisted patterning.[9] Among these, the most reliable technique defining the exact positions of the nanowires still remains to be e-beam lithography.[10] Although, it provides impressive precision, the process is time-consuming on a large (wafer) scale and unable to satisfy the condition of cost effectiveness. Hence, e-beam lithography is good for prototype device processing but not suitable for cheap nanowire device fabrication on a large scale. There are several other nanolithographic methods that attempt structural alignment for device production, but up until now, these routes could be utilized with only very limited success.[11] The most recent techniques for subwavelength photolithography such as immersion lithography and even X-ray lithography still require expensive tools for realization.[12] A solution for this positioning and nanostructuring problem could be the use of a technique that can achieve a resolution similar to e-beam lithography, but in a more efficient manner by way of combining the latest nanotechnologies with the current microsystems techniques.

Phase shift lithography (PSL), a simple approach, is one of the resolution enhancing techniques, which is still based on conventional optical lithography.[13] The concept was originally invented due to the increasing demand of size reduction in the electronics industry. The principle behind the PSL is based on destructive interference and is used to generate subwavelength dark lines as a lithography pattern. The resulting PSL pattern can vary depending on factors such as mask material, photoresist, and wavelength of the UV source. The accomplishment of this method yields impressive results down to 25 nm which is now already applied to industrial electronic device fabrication and nanotechnology.[14] In this work, we will demonstrate the use of phase shift lithography as a cost-effective approach for nanowire positioning on large scales either by etching Si or using structured Au dot patterns for the vapor solid (VS) growth of ZnO nanowires.

Realization of Large Scale Nanopatterning via Phase Shift Lithography. In the case of phase shift lithography, the intensity of light passing through a transparent element is modulated in the near field depending on the depth of the steps and the wavelength of the light source. In the past, several materials were used for the fabrication of the PSL masks such as PDMS, quartz, or glass.[12,15,16] We selected a glassy material as the material of
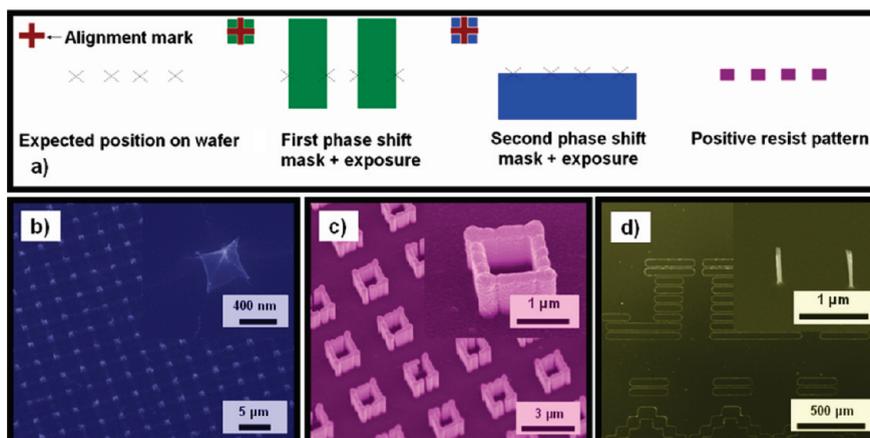
Figure 1. (a) Two-step exposure PSL for positioning NWs. With this technique, various nanostructures can be fabricated. As examples we selected (b) Si-based nanoneedles, (c) fencelike Si nanowire arrays in boxlike shape overgrown by ZnO demonstrating nanocontainers, and (d) an array of NWs prepared by PSL assist.

choice. The master mask for the desired pattern, i.e., a simple line pattern in our case, was fabricated on a UV transparent glass substrate by typical photolithography. After photolithography, the pattern was transferred into the glass substrate by reactive ion etching (RIE) to obtain the required step depth which follows the relation

$$d = \frac{\lambda}{2(n-1)} \quad (1)$$

where d is the step depth, n the refractive index of the mask material, and λ the wavelength of UV light source in the mask aligner. Fabrication of the phase shift pattern was realized similar to processes reported before.[17] However, instead of using one mask and crossing the mask by 90° for the second exposure, we simply designed two masks as shown in Figure (1a). Aligner marks were placed on the substrates as well as on the phase shift masks, both fitting well to each other. The fabrication of photoresist nanodot arrays (needed for selective nanowire growth) always requires a two-step exposure process. The first exposure defines the dark lines in the Y axis and the second one defines the dark lines in the X axis. Both exposures were done in sequence, and the samples were developed afterward in the conventional way. Along the interception points, photoresist nanodots appeared in the case of positive photoresist and nanoholes in the case of negative photoresist. With this technique, a very precise pattern can be produced on 4 in. wafers. The method can be used to fabricate various kinds of nanostructures. As a demonstration, an array of sharp nanoneedles can be observed (Figure 1b). These millions of nanoneedles have rectangular bases of 400 nm, but the tips are well below 20 nm. In Figure 1c, a boxlike structure is shown. This is achieved by arranging Si nanowires like a fence, next to each other, and then coating the structure by atomic layer deposition (ALD) with ZnO, resulting in square containers. In Figure 1d, Si nanowires patterned in large arrays on a 4 in. wafer (the fabrication process will be explained below) are shown. This gives an impression about the variety of nanostructures which can be produced for applications in the fields of photovoltaics, biology, chemistry, and electronics.

Fabrication of Si and ZnO Nanowire Arrays. ZnO NWs are typically grown by several methods such as pulsed laser deposition and solution-phase and vapor-phase deposition.[18−20] The growth commonly requires well-defined nucleation sites based on metal catalyst dots (i.e., Au) or homocatalysts (i.e., Zn or ZnO). Au dots are the most often used nucleation sites for the growth of ZnO as well as for many other semiconductor NWs. For the Au dots, a thickness of 20 nm is often chosen for the thermal evaporation process. If a thin (nonstructured) Au film is used for the growth of nanowires, at high temperatures, the film breaks into an infinite number of nanoclusters. From these self-arranged nanoclusters, very dense arrays of disordered nanowires can be grown. The crawling growth and a fractured wall structure below the desired ZnO NWs can also be observed.[21] ZnO NWs grown by using such thin Au films always form a forest-like nanostructure which is undesired for most applications. Especially, the spongelike film growth beneath the nanowires is a serious issue. For the vertical device technology, well-separated nanowires without the underlying film is a must.

With the phase shift lithography process, fabrication of patterned Si NWs and Au dots for ZnO NW growth were performed. Figure 2 represents the schematic process flow used in our experiments. In Figure 2a, the top-down process is demonstrated, resulting in aligned Si NWs by combining phase shift lithography with the conventional etching process. The bottom-up growth of vertical ZnO NW pattern is demonstrated in Figure 2b using a GaN (0001) film grown on sapphire as suitable substrate. For more details please see the method summary provided below. The results from a phase shift pattern of the etched Si NWs and selectively grown ZnO NWs are shown in Figure 3. Clearly, both the Si NWs and the ZnO NWs can be patterned into large areas. The remaining "resist caps" on Si NWs (Figure 3a), display the degree of anisotropy of the inductively couple plasma (ICP) etching process. The diameters of the Si NWs range from 100 to 200 nm with an average size of 150 nm, but this number can be further reduced. Although arrays of etched Si NWs might not be suitable for high end applications due to the defect properties of etched surfaces, our results demonstrate the possibility of the fabrication of Si NWs by combining phase shift technique and VLS growth down to very small diameters in the desired pattern. Pattern arranged VLS Si wires are studied for the use in photovoltaic devices.[22]

The grown ZnO NWs have the same pattern arrangement as the etched Si NWs. The GaN substrate is not perfectly flat as can be seen by the surface roughness below the ZnO NWs
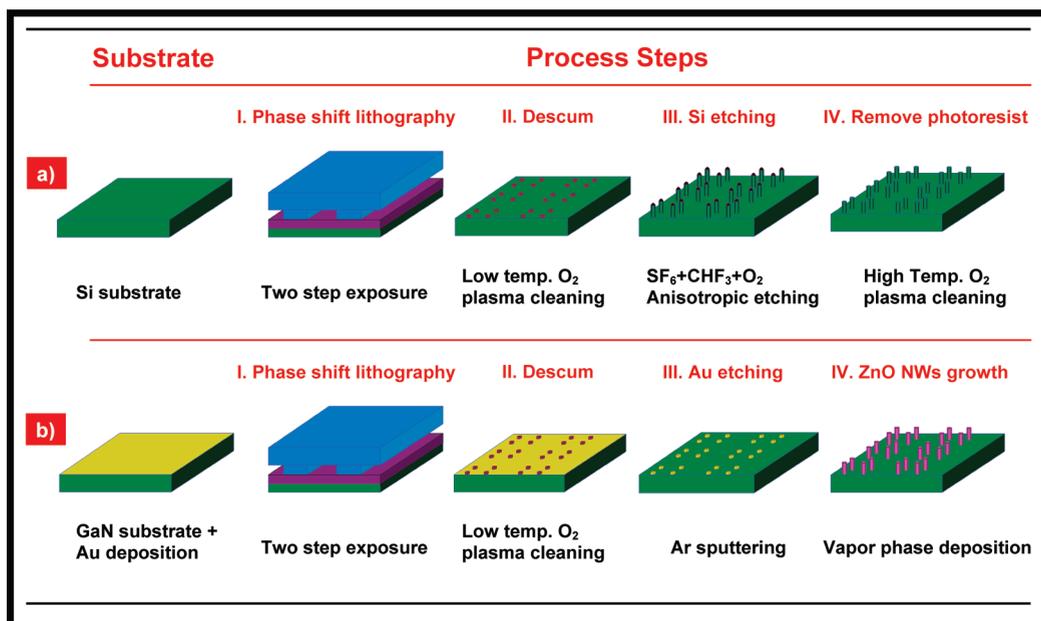
Figure 2. The fabrication processes of (a) Si etched NWs and (b) ZnO grown NWs.
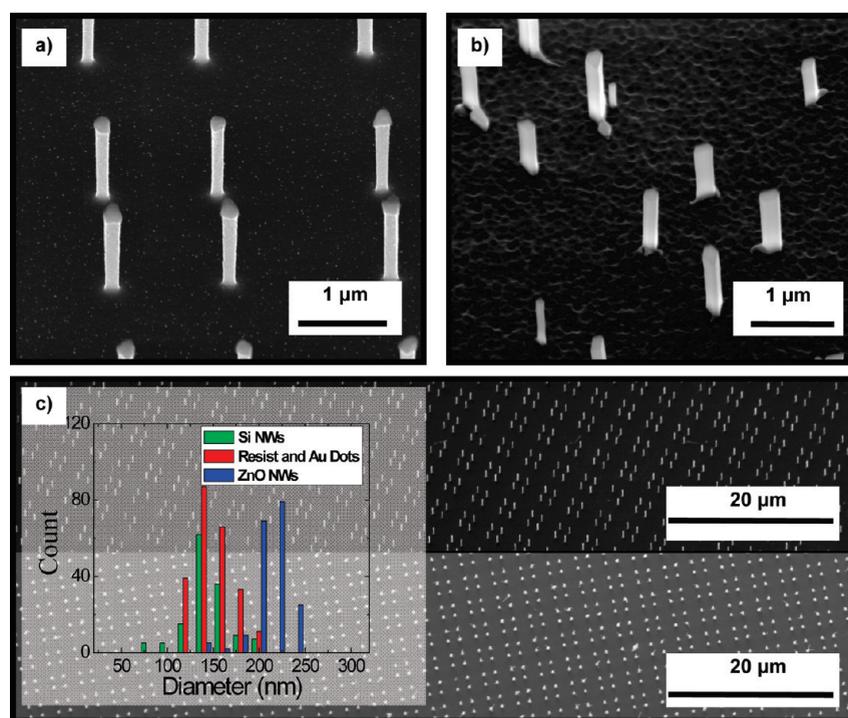

Figure 3. SEM picture of (a) Si NWs pattern and (b) ZnO NWs pattern based on PSL patterning. (c) Comparing the size distribution of pattern ZnO NWs and pattern Si NWs with the original resist size or Au size. The pattern Si NWs (top) and ZnO NWs (bottom) on large scale are shown.

(Figure 3b). Figure 3c compares the distribution of the as prepared resist dot size with the resulting etched Si and grown ZnO nanowires. Sharing the same pattern approach, the size of the grown ZnO NWs was found to be always bigger than the etched Si NWs. The size of Si NWs was in very good agreement with the resist dot size after the anisotropic etching process. However, in the case of ZnO NWs, the size is controlled by the self-organized vapor phase growth process, which is governed by oxygen concentration and substrate temperature and pressure in

a rather complex manner. This results in nanowires with sizes ∼40% larger than the Au dot diameter. The deviation strongly depends on the source/substrate temperature combination as was previously shown for CdSe nanowires.[23]

After the feasibility of large nanowire arrays was confirmed, the next step was to fabricate a device based on the above prepared NWs. As shown in Figure 4a, the Si NWs are buried under a sacrificial photoresist layer. Next, the photoresist was slowly removed by O_2 plasma to reopen half of the length of the Si NWs.
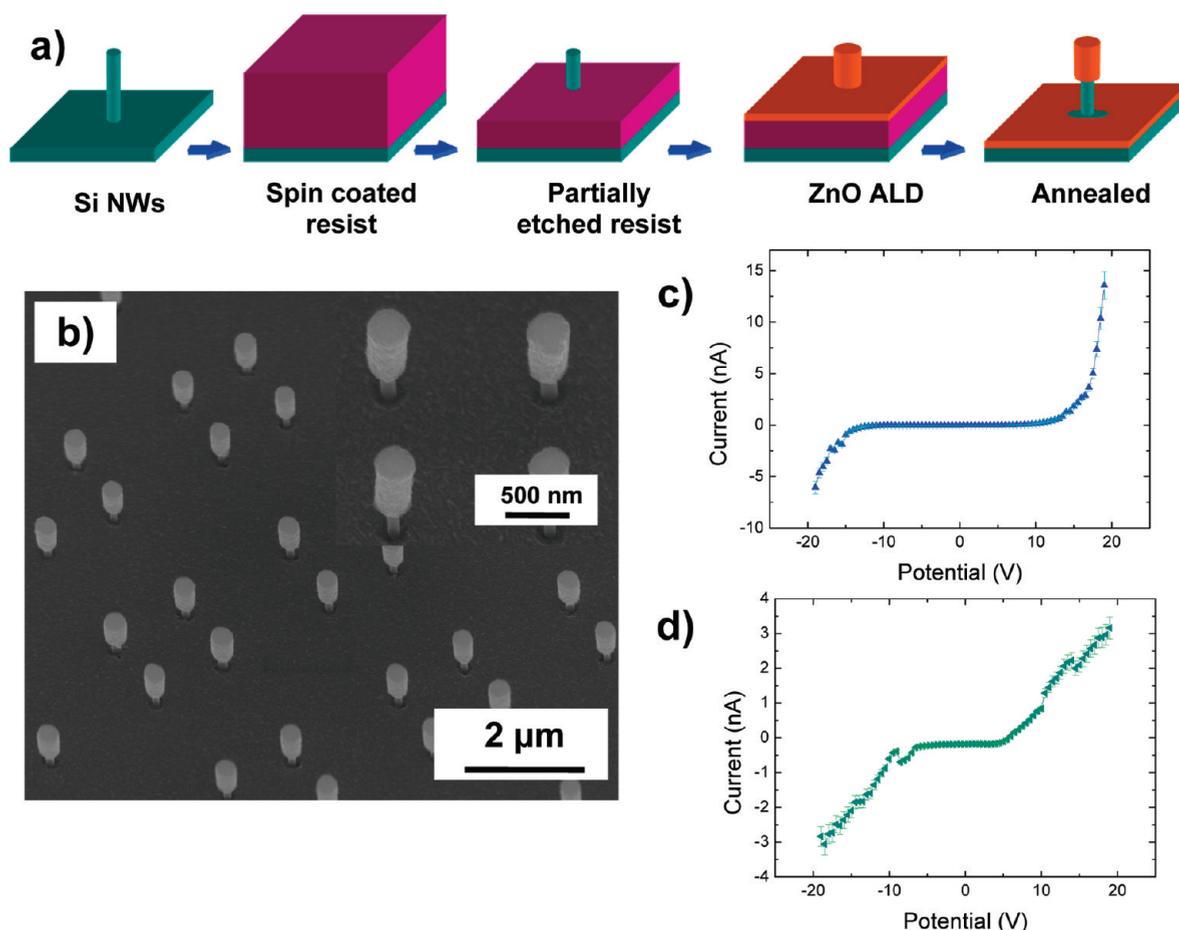
Figure 4. (a) Fabrication process of Si/ZnO NW diodes. (b) SEM pictures of the resulting Si/ZnO NW diodes. The inset shows four diodes in more detail. (c, d) $I-V$ characteristics of Si/ZnO NW diodes with high (c) and low (d) carrier concentration of the etched Si. As expected, a better rectify behavior is measured for the diode based on highly doped Si.

ALD was used to homogeneously cover the surface of the still half buried Si NWs with a 80 nm ZnO film resulting in domelike ZnO nanoshells over the Si NWs. The remaining photoresist was thermally removed by annealing at 400 °C. A post-thermal treatment process was carried out to improve the ZnO/Si junction quality forming a heterojunction diode. Figure 4b demonstrates the resulting array of vertically patterned Si/ZnO nanowire heterojunction diodes (Si/ZnO NW diodes) on the Si substrate. The inset of Figure 4c shows four of the arranged devices in more detail.

The Si/ZnO NW diodes were characterized by electrical measurements. $I-V$ measurements of a single Si/ZnO NW diode were carried out inside a high-resolution scanning electron microscope (SEM-JEOL JSM 6400F) equipped with a pair of nanomanipulators (Kleindiek) with electrically contacted platinum tips. The respective measurements are shown in parts c and d of Figure 4. Because ZnO is naturally n-doped, we used Si substrates with different p-doping levels to show its influence on the resulting diode characteristics. An Anderson-based model was applied for the Si/ZnO NW diodes as an ideal case approximation.[24] The space charge region can be characterized by

$$X_1 = \left[\frac{2N_A\varepsilon_1\varepsilon_2(V_{bi} - V)}{qN_D(N_D\varepsilon_1 + N_A\varepsilon_2)} \right]^{0.5} \quad (2)$$

for the space charge region on n-type side, and

$$X_2 = \left[\frac{2N_D\varepsilon_1\varepsilon_2(V_{bi} - V)}{qN_A(N_D\varepsilon_1 + N_A\varepsilon_2)} \right]^{0.5} \quad (3)$$

for the space charge region on p-type side. X_1 and X_2 are the depletion regions in the n-type and p-type semiconductor, q is the elementary charge, N_D is the donor concentration in n-type, N_A is the acceptor concentration in p-type, ε_1 and ε_2 are the dielectric constant of n- and p-type semiconductor, respectively, V_{bi} is the built-in potential, and V is the potential across the p-n junction.

The $I-V$ characteristics of the Si/ZnO NW diode mainly depend on the material properties as shown in eqs 2 and 3. The carrier concentration of n-type ZnO prepared by ALD was reported to be in the range of 10^{18} cm^{-3},[25] but will vary depending on preparation conditions and heat treatment. For the p-type Si NWs, the carrier concentration was varied from 10^{15} to 10^{18} cm^{-3} depending on the base substrate. At zero potential, and for a high carrier concentration of the Si NWs, the space charge region was in the range of 1 nm in the Si NW and 10 nm in the ZnO shell. With a low carrier concentration of the Si NWs, the space charge region becomes very large (several micrometers) in Si but almost vanishes in ZnO representing the case
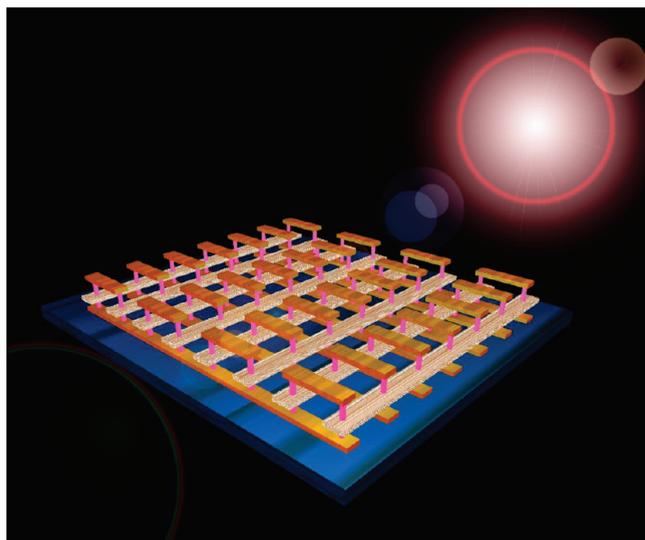
Figure 5. Memory device based on an array of NWs. One can realize the integration by other suitable techniques if the position of the nanowires is precisely defined.

of a one side abrupt junction. Hence, the depletion zone consumes almost the whole area of the Si nanowire.

On the basis of the model by Liou et al.[26] the capacitance of the heterojunction was proposed to be

$$C = \frac{\varepsilon_1 \varepsilon_2}{X_1 \varepsilon_2 + X_2 \varepsilon_2} + \int_{-X1}^{X2} [\partial n(\text{or} \rightarrow \partial p)/\partial V] \, dx = C_D + C_F \tag{4}$$

where n is the electron concentration, C_D, the capacitance which results from the change of the free carrier charges at the edges of the space-charge region, and C_F represents the change of the free-carrier charges in the volume of the space-charge region. From eq 4, a higher capacitance is expected for a Si/ZnO NW diode based on highly doped Si; hence, the breakthrough potential is expected to be higher in the Si/ZnO NW diode. The single nanowire based Si/ZnO device (highly doped Si) shows unequal currents between forward and reverse bias. The forward current yields a higher current at 20 V, while the cut-in and breakthrough potentials are the same at 14 V. The single Si/ZnO NW devices with a low carrier concentration of the Si shows an $I-V$ characteristic with a rather high unexpected noise and an equal current for both forward and reverse bias at 20 V which indicates bad rectification. The cut-in potential and breakthrough potentials are 5 and 7 V, respectively. As expected, single Si/ZnO NW diodes based on highly doped Si have a comparatively high output current and higher breakthrough potential than Si/ZnO NW diodes with a lower carrier concentration, i.e., low doping level of Si. We expect that with the presented simple technology here, various kinds of vertical semiconductor nanowire based devices can be produced. Figure 5 shows a scheme representing the future prospect of a memory circuit consisting completely of nanowire based transistors. The semiconductor nanowire device arrays can be incorporated into an integrated circuit via conventional, well-established fabrication techniques where the bit and word lines are placed accurately.

In summary, we demonstrated phase shift lithography as a powerful tool to pattern resist and Au layers to form dot arrays for applications. In combination with nanowire growth or conventional etching, we demonstrated the use of this technique to pattern or define the positions of NWs on large areas enabling reliable nanowire fabrication. Resist dots for Si NW etching as well as the transfer to Au nuclei for ZnO NW growth combined with the respective etching or growth processes demonstrated the feasibility of top-down as well as bottom-up nanowire positioning based on PSL.

The fabrication of Si/ZnO NW heterojunction diodes was selected as the prototype device and an example of device fabrication in large arrays. The measured $I-V$ characteristics of individual Si/ZnO NW diodes demonstrated not only the feasibility of the device fabrication process but also the controlled change of device properties. The reported, patterned fabrication of Si NWs and ZnO NWs in this article enable the integration of nanostructures into microelectronic circuits. The simple and cost-effective processes used here give the possibility for mass production of semiconductor NWs. Vertical semiconductor NW devices can be utilized in many applications such as gas sensing, biosensors, general purpose integrated circuits, photovoltaic, and many more.

■ ASSOCIATED CONTENT

ⓢ Supporting Information. Additional information regarding preparation of the phase shift pattern, ZnO vapor phase deposition, the ZnO/Si heterojunction system with Pt contact. This material is available free of charge via the Internet at http://pubs.acs.org.

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■ ACKNOWLEDGMENT

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